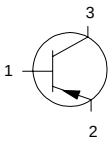
SOT-23 Formed SMD Package **CMBT5400**

HIGH VOLTAGE TRANSISTOR

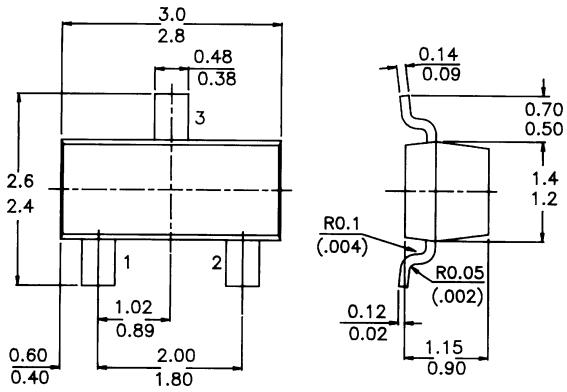
P–N–P transistor

Marking
CMBT5400 = K2

Pin configuration
1 = BASE
2 = EMITTER
3 = COLLECTOR



PACKAGE OUTLINE DETAILS
ALL DIMENSIONS IN mm



ABSOLUTE MAXIMUM RATINGS

Collector–base voltage (open emitter)	$-V_{CBO}$	*max.*	*130*	*V*
Collector–emitter voltage (open base)	$-V_{CEO}$	*max.*	*120*	*V*
Emitter–base voltage (open collector)	$-V_{EBO}$	*max.*	*5*	*V*
Collector current (d.c.)	$-I_C$	*max.*	*500*	*mA*
Total power dissipation at T_{amb} = 25°C	P_{tot}	*max*	*250*	*mW*
D.C. current gain				
$-I_C$ = 10 mA; $-V_{CE}$ = 5 V	h_{FE}	*min.*	*40*	
		max.	*180*	

RATINGS *(at T_A = 25°C unless otherwise specified)*
Limiting values

Collector–base voltage (open emitter)	$-V_{CBO}$	*max.*	*130*	*V*
Collector–emitter voltage (open base)	$-V_{CEO}$	*max.*	*120*	*V*
Emitter–base voltage (open collector)	$-V_{EBO}$	*max.*	*5*	*V*
Collector current (d.c.)	$-I_C$	*max.*	*500*	*mA*

Total power dissipation at T_{amb} = 25°C	P_{tot}	*max*	*250*	*mW*
Storage temperature	T_{stg}	*–55 to +150*		*° C*
Junction temperature	*Tj*	*max.*	*150*	*° C*

THERMAL CHARACTERISTICS

T_j = P ($R_{th\ j–t}$ + $R_{th\ s–a}$) + T_{amb}

Thermal resistance				
from junction to ambient	$R_{th\ j–a}$		*200*	°C/mW

CHARACTERISTICS *(at T_A = 25°C unless otherwise specified)*

Collector–emitter breakdown voltage				
$–I_C$ = 1 mA; I_B = 0	$–V_{(BR)CEO}$	*min.*	*120*	*V*
Collector–base breakdown voltage				
$–I_C$ = 100 µA; I_E = 0	$–V_{(BR)CBO}$	*min.*	*130*	*V*
Emitter–base breakdown voltage				
$–I_E$ = 10 µA; I_C = 0	$–V_{(BR)EBO}$	*min.*	*5*	*V*
Collector cut–off current				
$–V_{CB}$ = 100 V; I_E = 0 V	$–I_{CBO}$	*max.*	*100*	*nA*
Emitter cut-off current				
$–V_{EB}$ = 3V; I_C = 0	$–I_{EBO}$	*max.*	*50*	*nA*
Output capacitance at f = 1 MHz				
I_E = 0; $–V_{CB}$ = 10 V	C_c	*max.*	*6*	*pF*
Saturation voltages				
$–I_C$ = 10 mA; $–I_B$ = 1 mA	$–V_{CEsat}$	*max.*	*0.2*	*V*
	$–V_{BEsat}$	*max.*	*1*	*V*
$–I_C$ = 50 mA; $–I_B$ = 5 mA	$–V_{CEsat}$	*max.*	*0.5*	*V*
$–I_C$ = 50 mA; $–I_B$ = 5 mA	$–V_{BEsat}$	*max.*	*1*	*V*
D.C. current gain				
$–I_C$ = 1 mA; $–V_{CE}$ = 5 V	h_{FE}	*min.*	*50*	
$–I_C$ = 10 mA; $–V_{CE}$ = 5 V	h_{FE}	*min.*	*40*	
		max.	*180*	
$–I_C$ = 50 mA; $–V_{CE}$ = 5 V	h_{FE}	*min.*	*40*	
Noise figure at R_S = 1 kΩ				
$–I_C$ = 200 µA; $–V_{CE}$ = 5 V				
f = 10 Hz to 15.7 kHz	*NF*	*max.*	*8*	*dB*

Customer Notes

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished on the CDIL Web Site/ CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

CDIL is a registered Trademark of
Continental Device India Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone + 91-11-2579 6150, 5141 1112 Fax + 91-11-2579 5290, 5141 1119
email@cdil.com www.cdilsemi.com